IN THE ABSTRACT:

Please AMEND the Abstract as indicated (marked up copy and clean copy at end of Amendment).

IN THE SPECIFICATION:

Please REPLACE the paragraph beginning at page 2, line 10, with the following paragraph:

A2

The instruction execution units EU0 to EUn execute the basic instructions, and notify the instruction issue unit 3 of the end of the execution. The register unit 5 supplies data to the instruction execution units EU0 to EUn, if necessary, and holds the execution results of the instruction execution units EU0 to EUn. The externally connected memory 7 stores an instruction word string to be executed in the parallel processor 10. The memory 7 also stores necessary data for the execution units EU0 to EUn to execute instructions, and data as the execution results.

Please REPLACE the paragraph beginning at page 2, line 22, with the following paragraph:

A3

FIG. 2 shows the formats of instruction words to be supplied to a parallel processor having four instruction execution units EU0 to EU3. As shown in FIG. 2, each instruction word is made up of a basic instruction EI and a do-nothing instruction NOP. If the number of basic instructions contained in one instruction word to be executed in parallel is smaller than the number of the instruction execution units EU0 to EU3, the proportion of do- nothing instructions is large.

Please REPLACE the paragraph beginning at page 3, line 10, with the following paragraph:

A4

With the super scalar technique, there is also a problem that a large-scale circuit is needed to increase the number of instructions to be executed in parallel.

Please REPLACE the paragraph beginning at page 9, line 19, with the following paragraph:

A5

FIG. 5 shows the formats of instruction words to be supplied to the parallel processors of the first embodiment. Each instruction word is made up of one or more basic instructions EI and at least one of instruction word delimiting fields 0 and 1. The basic instruction word length is either 1 or 2. The upper row of FIG. 5 indicates an instruction word having a basic instruction word length of 2, consisting of a basic instruction word made up of an instruction word delimiting field 0 and a basic instruction EI, and another basic instruction word made up of an instruction word delimiting field 1 and a basic instruction EI. The lower row of FIG. 5 indicates an instruction word having a basic instruction word length of 1, consisting of an instruction word delimiting field 1 and a basic instruction EI.

Please REPLACE the paragraph beginning at page 10, line 20, with the following paragraph:

A6

Based on the instruction word delimiting fields 0 and 1 contained in the instruction words supplied from the cutting unit 316, the instruction issue unit 72 recognizes each basic instruction EI, and issues each basic instruction EI selectively to one of the instruction execution units EU0 and EU1 via the selectors 355 and 356. Accordingly, if a basic instruction EI following an instruction word delimiting field 0 is issued to the instruction execution unit EU0, a basic instruction EI following an instruction word delimiting field 1 is issued to the instruction execution unit EU1. The selectors 355 and 356 are controlled by the control unit 370. When the execution of one instruction word is completed, the corresponding basic instruction EI is supplied to the instruction execution units EU0 and EU1 via the selectors 355 and 356.

Please REPLACE the paragraph beginning at page 14, line 5, with the following paragraph:

A7

As described so far, the parallel processor 21 of this example can have the same effects as the parallel processor 20 of Example 1, and efficiently and accurately performs the parallel processing of the basic instructions EI. Thus, more reliable operations can be achieved.

Please REPLACE the paragraph beginning at page 16, line 26, with the following paragraph:

A8

For simplification of the drawing, only two instruction passages from an instruction register 348 to the two instruction execution units LU0 and IUO are shown in FIG. 8. However, it should be understood that there are the other instruction passages to the instruction execution units IU1, FU0, FU1, and BU0, as shown in FIG. 7.

Please REPLACE the paragraph beginning at page 18, line 22, with the following paragraph:

A9

FIG. 10 is a circuit diagram of the conversion unit 115 shown in FIG. 8. As shown in FIG. 10, the conversion unit 115 comprises transmission lines L1 and L2, BI detectors BD1 and BD2, FI detectors FD1 and FD2, II detectors ID1 and ID2, LI detectors LD1 and LD2, buffers 155 to 158, AND gates 163 to 166, 185, and 186, exclusive OR gates 187 to 190, selectors 209 to 212, and OR gates 199 to 202.

Please REPLACE the paragraph beginning at page 19, line 7, with the following paragraph:

A10

The FI detector FD1 is connected to the transmission line L1, and the FI detector FD2 is connected to the transmission line L2. The buffer 156 is connected to the FI detector FD1, and the AND gate 164 is connected to the FI detectors FD1 and FD2. The two input terminals of the exclusive OR gate 187 are connected to the input node and the output node, respectively, of the buffer 156. The two input terminals of the exclusive OR gate 188 are connected to the output node of the AND gate 164 and the FI detector FD2, respectively. The AND gate 185 is connected to the two exclusive OR gates 187 and 188. The selector 210 is connected to the transmission lines L1 and L2, the buffer 156, and the AND gate 164. The OR gate 200 is connected to the buffer 156 and the AND gate 164.

Please REPLACE the paragraph beginning at page 21, line 24, with the following paragraph:

A10

As the second basic instruction FI is detected, the BI detector BD2, the II detector ID2, and the LI detector LD2 output non-detection signals of logic 0. Accordingly, the selectors 209, 211, and 212 do not select the second basic instruction transmitted through the transmission line L2. Since neither first nor second basic instructions to be execution by the instruction executed units LU0, IU0, IU1, and FU1 are detected, the effective bit V of logic 0 is outputted from each of the OR gates 201 and 202, and the AND gates 185 and 186.

Please REPLACE the paragraph beginning at page 22, line 26, with the following paragraph:

A11

The conversion unit 115 having the above structure operates in the same manner as the conversion unit 115 shown in FIG. 10. In the following, an operation of the conversion unit 115 in a case where an instruction word made up of basic instructions BI, FI, FI, and II is supplied to the conversion unit 115 will be described. First, the first basic instruction BI is transmitted through the transmission line L1. The BI detector BD1 then detects the basic instruction BI and supplies a detection signal of logic 1 to the buffer 159. At this point, each of the AND gates 167 to 169 outputs a logic 0 signal. In accordance with the detection signal supplied from the buffer 159, the selector 213 selects the first basic instruction BI and outputs the first basic instruction BI, that is an instruction to be executed by the instruction execution unit BU0, to the instruction issue unit 74. At the same time as the output of the first basic instruction BI, the OR gate 203 outputs the effective bit V of logic 1 in accordance with the detection signal supplied from the buffer 159. As the first basic instruction BI is detected, the FI detector FD1, the II detector ID1, and the LI detector LD1 output non-detection signal of logic 0. Accordingly, the selectors 214, 216, and 218 do not select the first basic instruction BI transmitted through the transmission line L1.

Please REPLACE the paragraph beginning at page 25, line 15, with the following paragraph:

A12

In this example, the instruction fetch unit 48 can also fetch an instruction word containing basic instructions that have already been arranged in accordance with the

A12

arrangement of the instruction execution units in advance. In such a case, the basic instructions are arranged in advance so that the circuit size required for rearranging the basic instructions in the instruction fetch unit 48 can be reduced.

Please REPLACE the paragraph beginning at page 30, line 12, with the following paragraph:

A13

For simplification of the drawing, only the instruction passages from an instruction register 351 to the two instruction execution units LU0 and IU0 are shown, and the other instruction passages to the instruction execution units IU1, FU0, FU1, and BU0 are omitted in FIG. 17. Likewise, only the two execution complete signals LUc and IUc0 are shown as signals to be supplied to the judgment unit 104, and the other execution complete signals are omitted in FIG. 17.

Please REPLACE the paragraph beginning at page 33, line 8, with the following paragraph:

A14

FIG. 21 shows the structures of the instruction fetch unit 53 and the instruction issue unit 79 of the parallel processor 27 shown in FIG. 20. The instruction fetch unit 53 and the instruction issue unit 79 have the same structures as the instruction fetch unit 50 and the instruction issue unit 76 shown in FIG. 15, except that the instruction issue unit 79 further includes the judgment unit 106 connected between an instruction register 353 and a control unit 376. Based on a supplied basic instruction, the judgment unit 106 determines whether or not a basic instruction to be issued has the data dependency or control dependency, or causes resource sharing. The judgment results are reported to the control unit 376. If the basic instruction to be issued has the data dependency or control dependency, or causes resource sharing, the instruction issue unit 79 issues the basic instruction only after the execution complete signals LUc and IUc0 are supplied.

Please REPLACE the paragraph beginning at page 34, line 29, with the following paragraph:

A15

As shown in FIGS. 22 to 27, parallel processors 28 to 33 in accordance with a third